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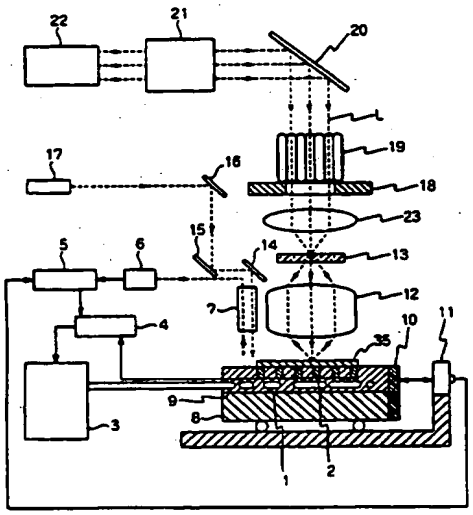
(54) Abstract Title
Forming a pattern on a semiconductor substrate including heating or cooling the substrate to adjust its size

(57) A light exposure method and device for forming a prescribed pattern on a semiconductor substrate 35 are described in which the size of a the semiconductor substrate is measured; any error between the measured size and the design size of the semiconductor substrate is determined; the semiconductor substrate is heated and/or cooled in order to correct the design size; and a prescribed pattern is exposed on to the semiconductor substrate. The light exposure device includes a light source for directing exposure light on to the semiconductor substrate; a detector 6 for detecting alignment marks formed on the semiconductor substrate; and a substrate position sensor 7 for detecting positional information for the semiconductor substrate when an alignment mark is detected. The light exposure device also includes a signal processing unit 5 for measuring the size of the semiconductor substrate from the output signal from the substrate position sensor, and for detecting an error between the measured size and the design size of the semiconductor substrate. The light exposure device also has a temperature regulating mechanism 1 for heating or cooling the semiconductor substrate on the basis of the output from the signal processing unit.

F I G. 1



F I G. 2

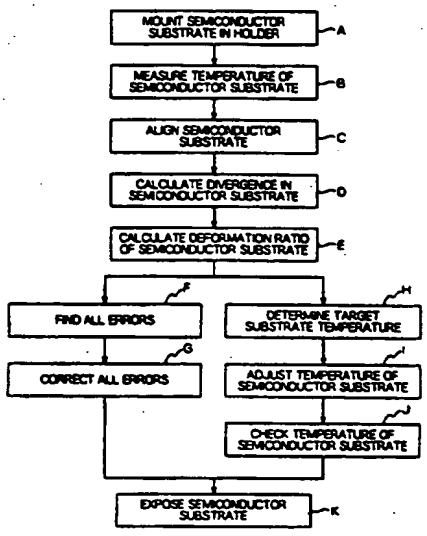


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FIG.1

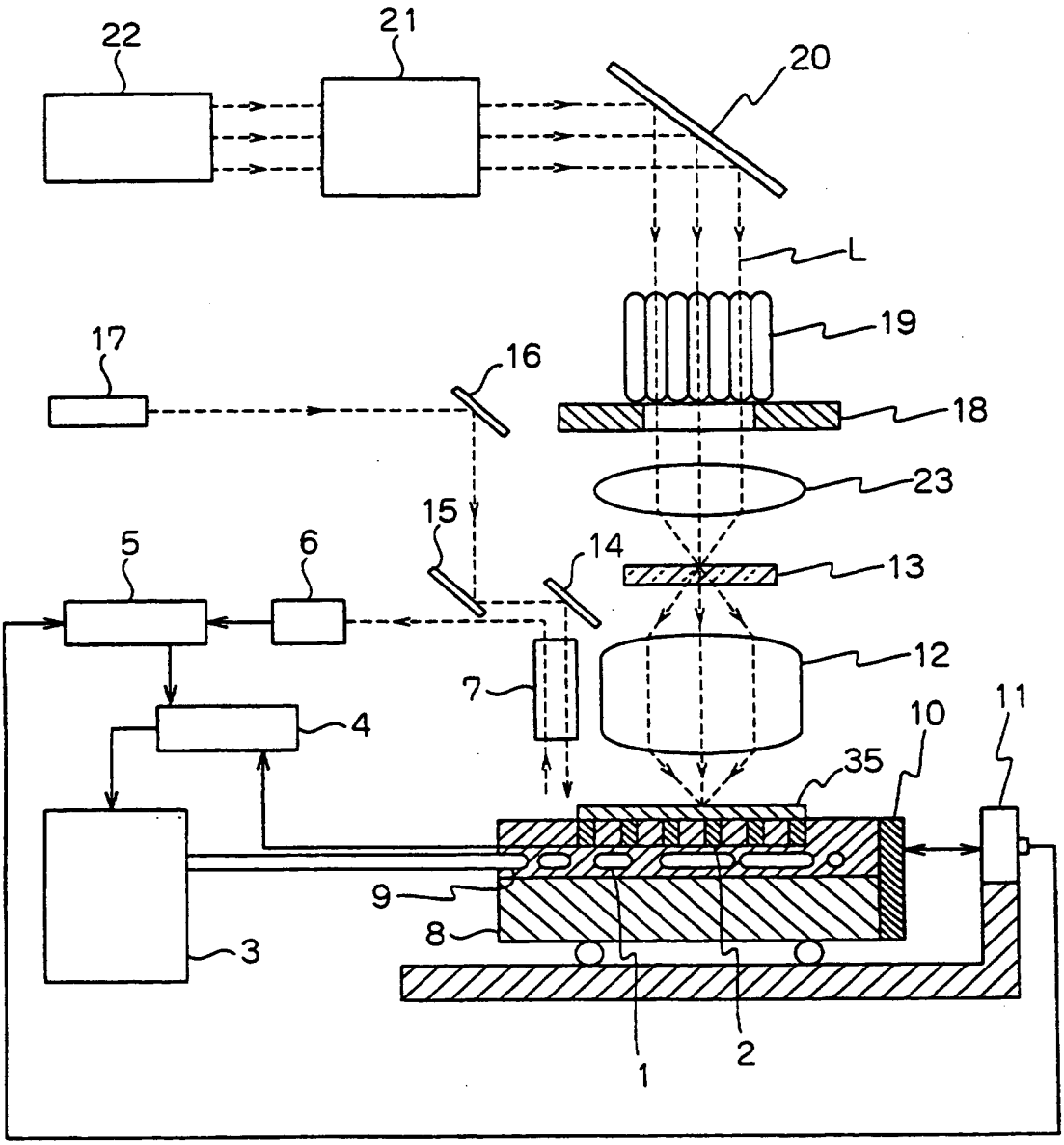


FIG.2

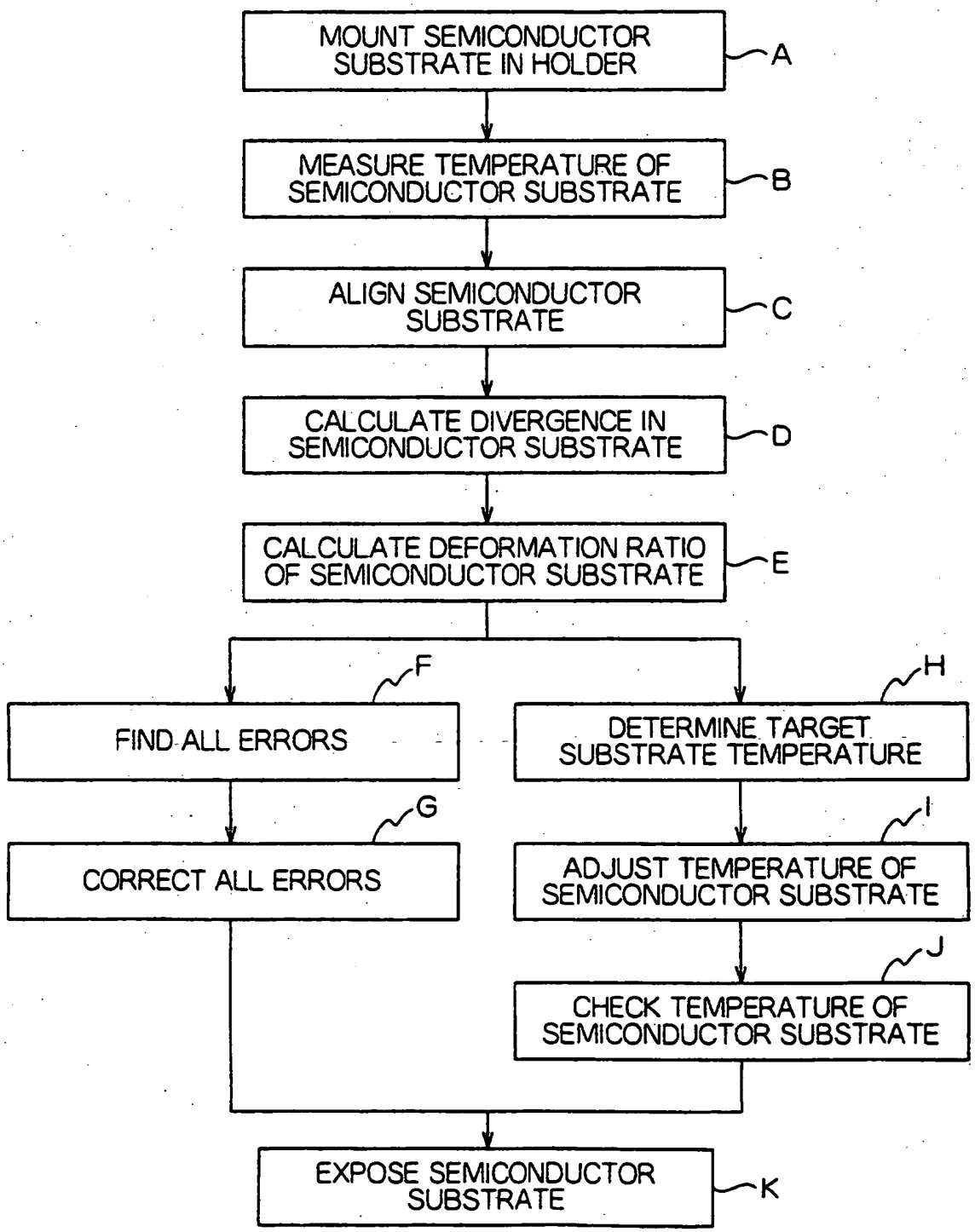


FIG.3

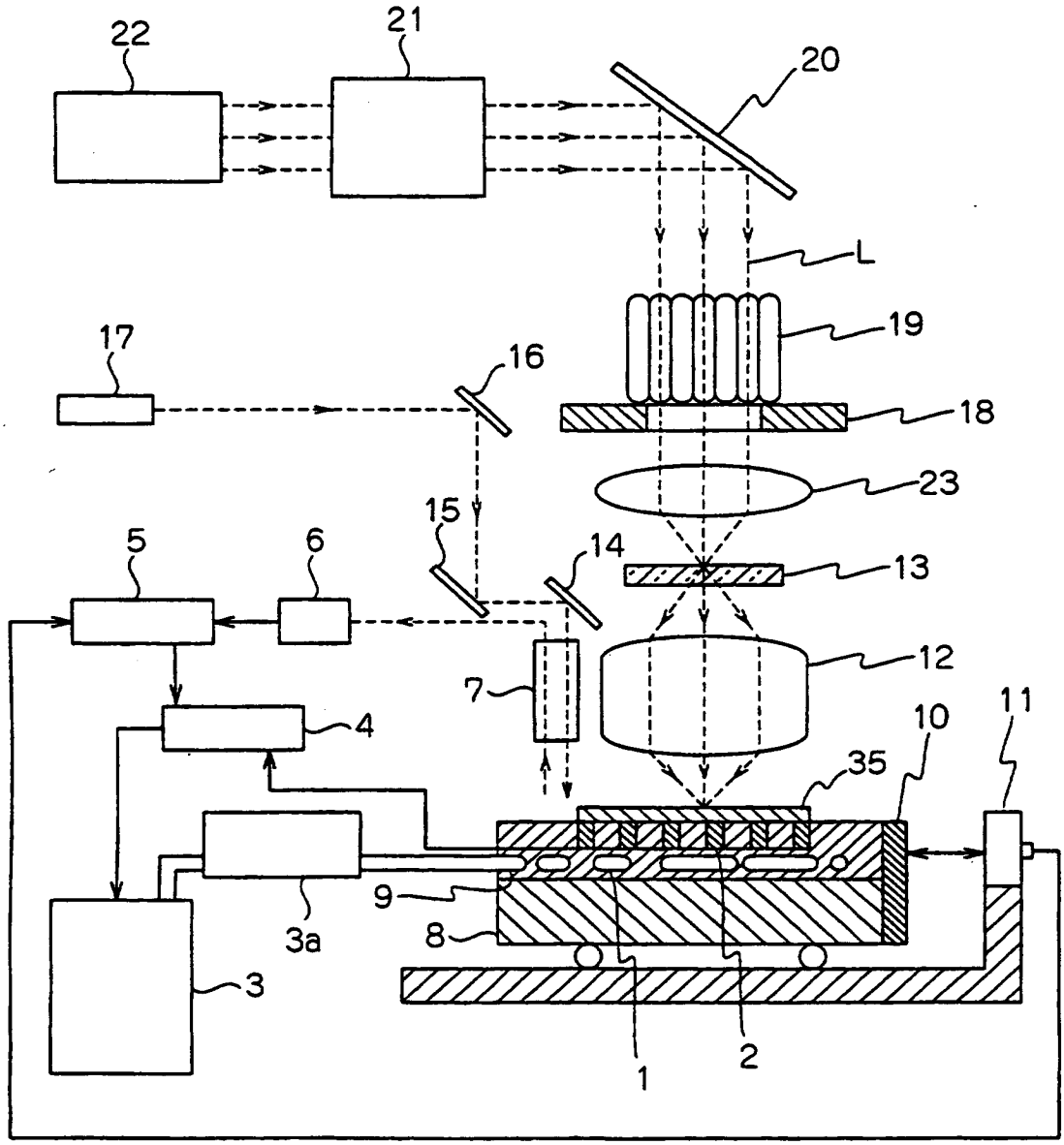


FIG.4

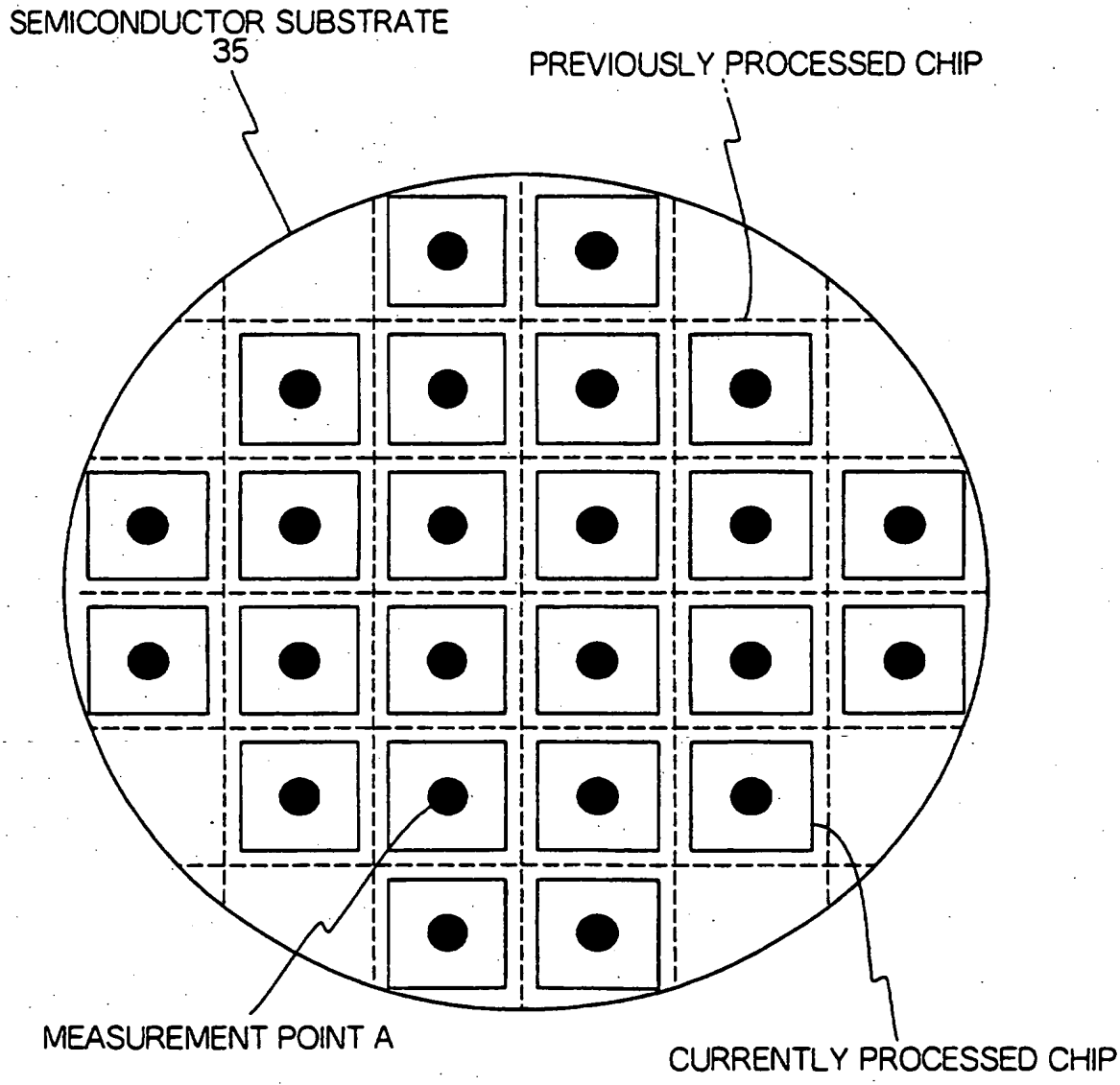


FIG.5

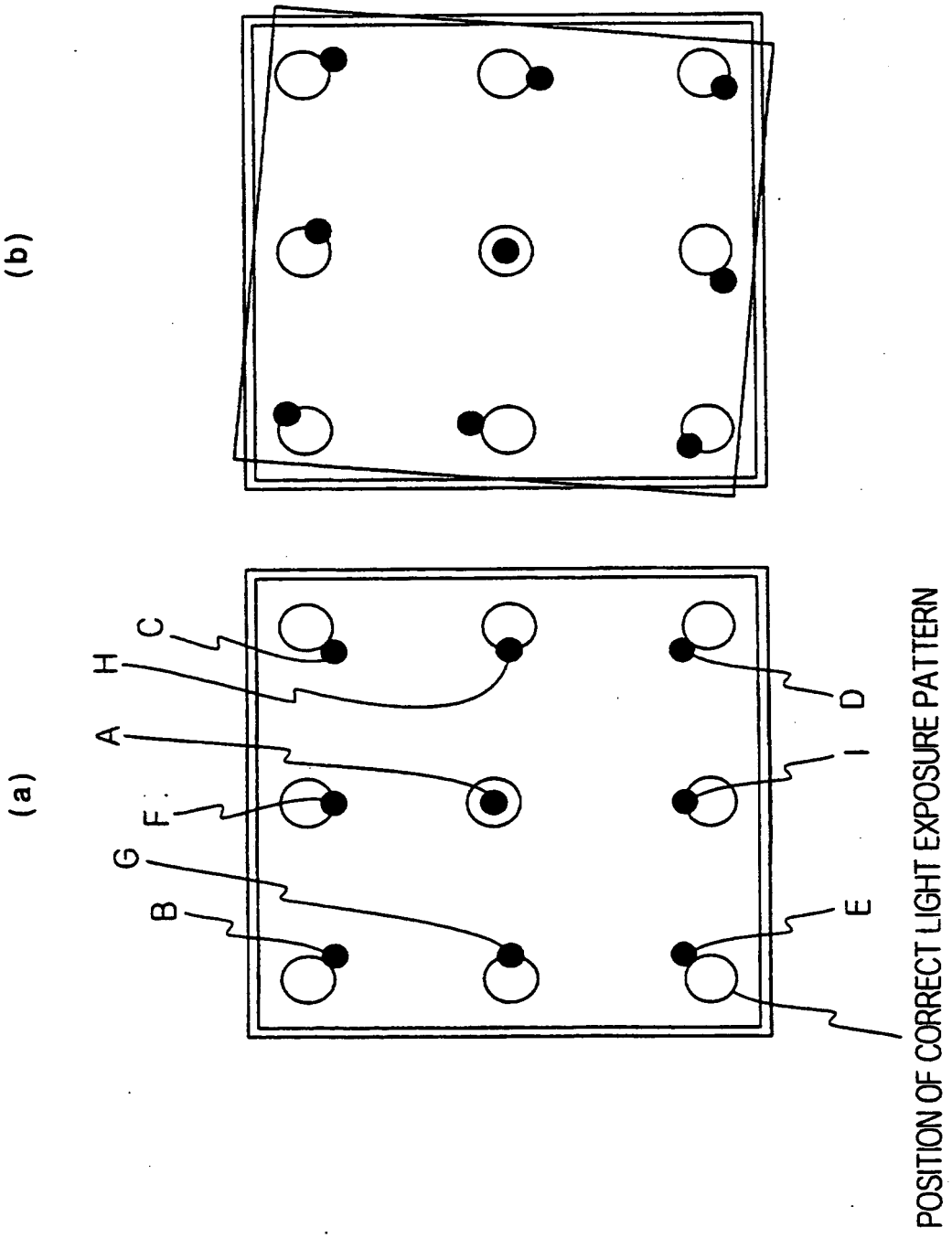
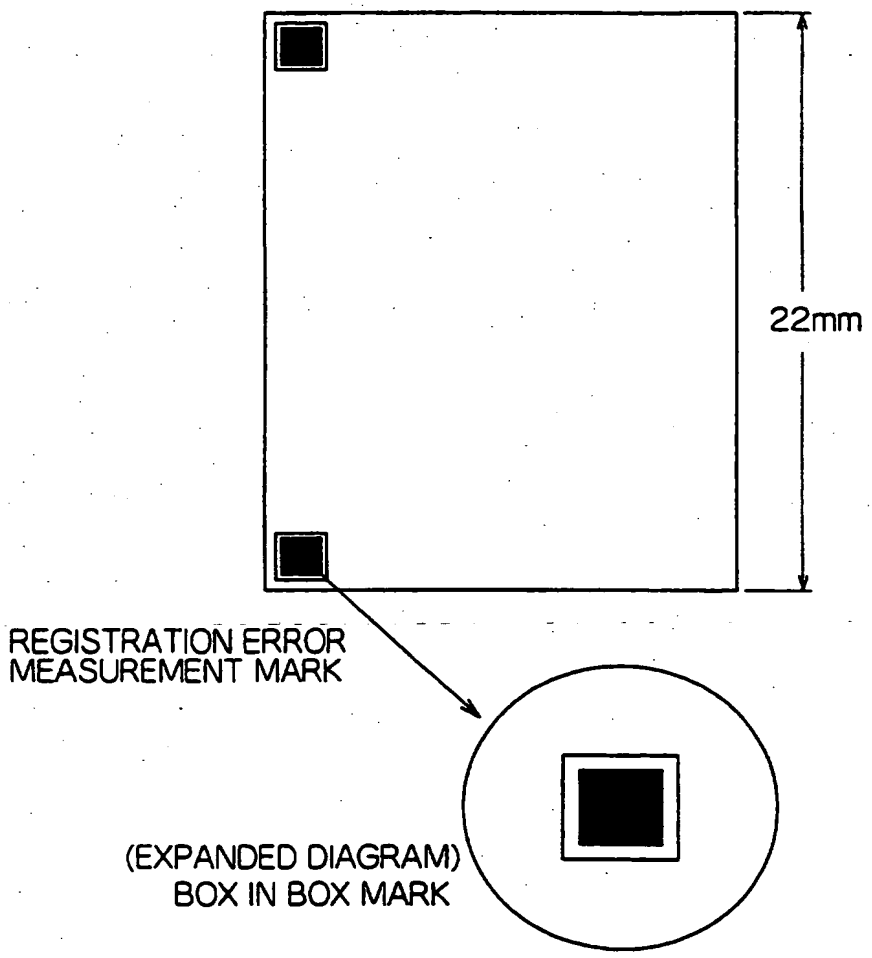


FIG.6



RELATIONSHIP BETWEEN FILM TYPE/FILM THICKNESS AND DEFORMATION OF SEMICONDUCTOR SUBSTRATE

FILM TYPE	FILM THICKNESS (A)	REGISTRATION ERROR WITHIN CHIP (μ m) (SUBSTRATE DEFORMATION / 22 mm)	SUBSTRATE DEFORMATION RATIO (ppm)
Si_3N_4	1000	−0.061	−2.77
Si_3N_4	2000	−0.106	−4.12
Si_3N_4	4000	−0.186	−8.45
SiO_2	4000	+0.043	+1.95
Si	10000	+0.197	+8.96
W	2000	−0.088	−4.00

(- : CONTRACTION ; + : EXPANSION)

FIG.7

FIG.8

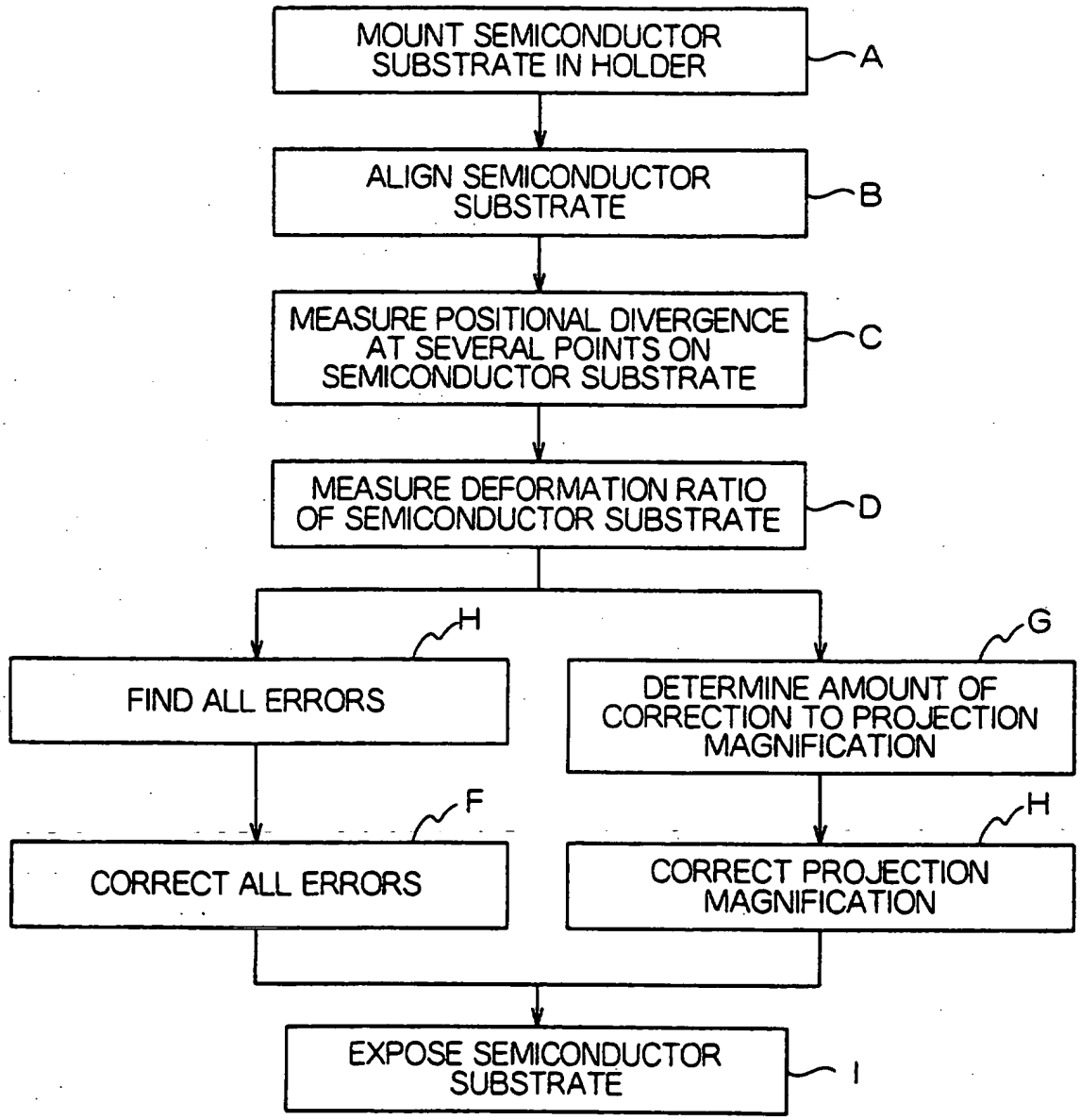
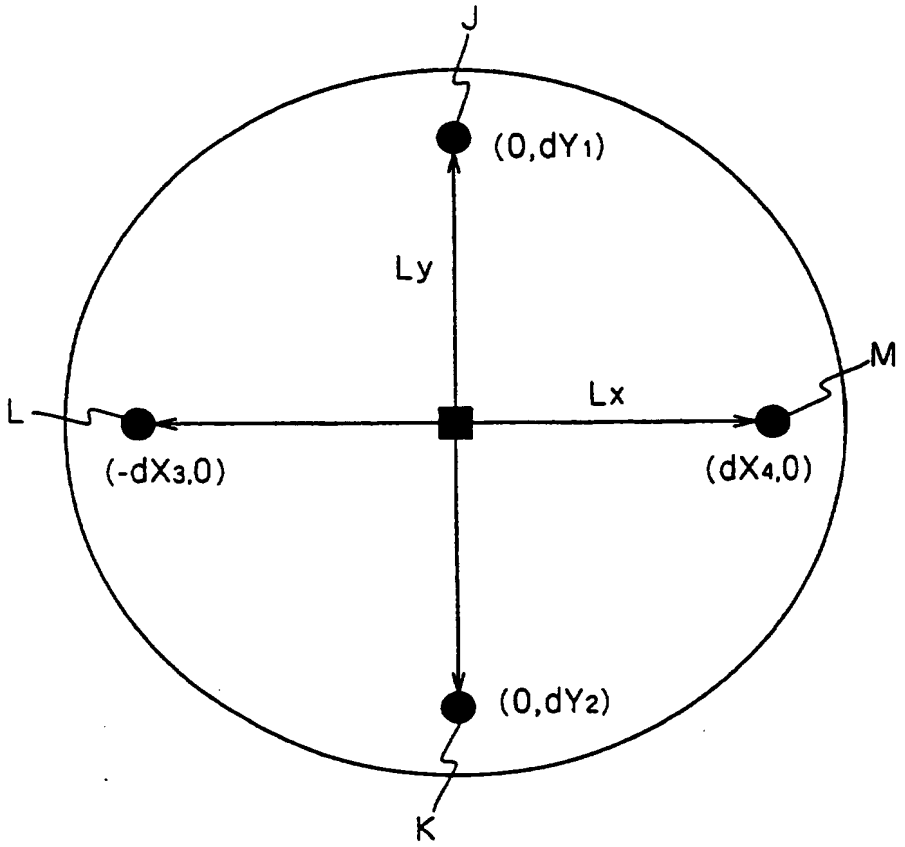


FIG.9



LIGHT EXPOSURE METHOD AND LIGHT EXPOSURE DEVICE

The present invention relates to a light exposure method and a light exposure device. A light exposure method and a light exposure device will be described below by way of example in illustration of the invention in which a circuit pattern formed on a mask is positioned over a semiconductor substrate and the circuit pattern is transferred.

In recent years, there has been a growing demand for increased density in semiconductor integrated circuits. Accordingly, there has been a trend towards further miniaturization of the pattern dimensions formed on to semiconductor integrated circuits. As miniaturization of the pattern dimensions advances, the registration accuracy required when overlaying a mask pattern on a semiconductor substrate becomes extremely strict.

In the fabrication of a semiconductor integrated circuit, the required registration accuracy is considered to be approximately 1/4 - 1/3 of the smallest dimension in the pattern to be formed. Below, the example of a DRAM (dynamic random access memory), which is a typical semiconductor integrated circuit, is used to describe this registration accuracy.

For example, in a DRAM having 64 MB (megabyte) capacity, the smallest dimension in the pattern formed onto the semiconductor substrate is about 0.35 μm. Therefore, the registration accuracy required in this case is approximately 0.10 μm. In a 256-MB DRAM, the smallest dimension in the pattern formed onto the semiconductor substrate is about 0.25 μm, and therefore the registration accuracy required is approximately 0.07 μm. Furthermore, in a DRAM having 1 GB (gigabyte) capacity, the smallest dimension in the pattern formed onto the semiconductor substrate is about 0.18 μm, and therefore the registration accuracy required is approximately 0.05 μm, which is extremely strict.

Here, there are many factors which affect the registration accuracy, for example, inherent deformation of the semiconductor substrate, or the inherent mechanical precision of the light exposure device. Moreover, there are various methods of classifying the registration accuracy. These include methods which distinguish between registration between chips and registration within a chip.

Reference will now be made to Figs. 4 to 9 of the accompanying drawings in which:-

Fig. 4 is a plan view of a semiconductor substrate which is helpful in describing the state of registration

between chips,

Fig. 5 shows plan views of a chip which is helpful in describing an error corresponding to a light exposure pattern in the case of registration within a chip: Fig. 5(a) showing a chip which has expanded with respect to a central alignment mark; and Fig. 5(b) showing a chip which has rotated about a central alignment mark,

Fig. 6 is a plan view of a semiconductor chip which is helpful in describing registration error within a chip,

Fig. 7 is a table indicating the relationship between film type and film thickness and the deformation of a semiconductor substrate in general semiconductor manufacture,

Fig. 8 is a flowchart which is helpful in describing a previously proposed method for correcting registration error within a chip, and

Fig. 9 is a diagram indicating alignment marks on a semiconductor substrate in a previously proposed example.

As shown in Fig. 4, for registration between chips, an alignment mark A for registration is previously formed on each chip. Thereupon, the aim is to overlay the mask pattern accurately on the semiconductor substrate 35 using these alignment marks A as a reference. Therefore, by concentrating on one chip only, the problem

arises of whether the mask pattern is overlaid accurately with respect to all of the plurality of alignment marks on the chips. In Fig. 4, the dotted lines indicate the regions exposed in the previous light exposure process, and the solid lines indicate the regions to be exposed in the next light exposure process. In Fig. 4, there is a large difference between the two, but this difference has been exaggerated in the diagram, and the actual difference is small.

Fig. 5(a) and Fig. 5(b), on the other hand, show approximate plan views of chips, for describing the registration within a chip. In registration within a chip, the aim is to overlay the mask pattern accurately with respect to points of some kind, or at least a plurality of alignment marks (A - I) within a chip. In Fig. 5(a), the mask pattern is accurately laid over the alignment mark A. However, it is not accurately laid over the other alignment marks B - H. In specific terms, in the case illustrated, the semiconductor substrate 35 is slightly smaller than the design dimensions. Moreover, in Fig. 5(b), the mask pattern is also laid accurately over the alignment mark A, but the other alignment marks B - H are shifted slightly in a rotational direction about the alignment mark A.

Registration accuracy between chips is principally

affected by the precision of the alignment sensors in the light exposure device, the stage accuracy, and the like. On the other hand, registration accuracy within a chip is principally affected by distortion (warping, twisting, fluctuation in magnification) in the lens used in the light exposure device, reticle rotation, and the like.

Methods for improving registration accuracy between chips and registration accuracy within a chip have both been the subjects of previous investigations. In particular, the focus has been on the very important problem of raising registration accuracy within a chip when fabricating highly integrated memories, such as a 256-MB DRAM. There are two principal reasons for this, as described below.

The first reason is the finding that when silicon nitride film, silicon oxide film, and polycrystalline film, etc. are formed on a semiconductor substrate, this produces deformation in the semiconductor substrate and hence leads to registration errors (Reference source: Akira IMAI et. al., SPIE Vol.2726, 1996, pp.104-112). The second reason is that if a semiconductor substrate expands or contracts by a certain ratio, then as the chip size gets larger, so the degree of error in registration within the chip also increases.

Fig. 6 is a plan view of a single chip for

describing registration error within a chip. An exposure pattern is overlaid on the chip by registering the solid black square with the square shape around the outside thereof. Fig. 7 shows a table of the relationships between the type of film and film thickness formed onto a semiconductor substrate and the amount of deformation of the semiconductor substrate. As shown in Fig. 6, this example of the error in registration within a chip caused by deformation of the semiconductor substrate is based on a semiconductor chip having a length of 22 mm in its longer direction. Two registration error measurement marks were placed in the longer direction of the chip and the degree of deformation produced in the semiconductor substrate by forming films of different materials was investigated. As shown in the table in Fig. 7, the corresponding results revealed that a maximum registration error of about 0.1 - 0.2 (μm) was produced within a chip, which is unsuitable for fabricating 256 MB DRAM memories or equivalent devices, if no correction of any kind is provided.

A method has previously been proposed in which the projection magnification is slightly adjusted in the projection and light exposure device for correcting registration error within a chip caused by deformation of the semiconductor substrate. This method will now be

described.

Fig. 8 is flowchart for use in illustrating the previously proposed method for correcting registration error within a chip, and Fig. 9 illustrates alignment marks formed on a wafer in order to calculate registration error. In this correction method, firstly, as shown at step A in Fig. 8, a semiconductor substrate coated with photoresist is conveyed to a light exposure device and mounted in a holder. Thereupon, at step B in Fig. 8, the semiconductor substrate is aligned. At step C, the amount of error at several points on the semiconductor substrate is measured by means of alignment sensors in the light exposure device. If, for example, the error is measured at four points (alignment marks J - M) near the outer perimeter of the semiconductor substrate, then using the following equations, it is possible to determine the deformation of the semiconductor substrate in the X direction and the Y direction at step D and step E.

Deformation in X direction: $(dX4 + dX3)/Lx$ (ppm) Eq. (1)

Deformation in Y direction: $(dy1 + dY2)/Ly$ (ppm) Eq. (2)

Here, dY1 is the error in the Y direction at alignment mark J, and -dY2 is the error in the Y direction at alignment mark K, and neither indicates co-ordinate values for the alignment marks. Furthermore,

-dX3 is the error in the X direction at alignment mark L, and dX4 is the error in the X direction at alignment mark M. The error is the divergence between the design value and the measured value when the centre of the semiconductor substrate is positioned accurately. Moreover, Ly is the distance between the alignment marks J and K, and Lx is the distance between alignment marks L and M. To simplify the description, the error in the X direction at alignment marks J and K has been taken as 0, and the error in the Y direction at alignment marks L and M has been taken as 0.

Finally, at step F, corrections are made to the shift, rotation, perpendicularity, reduction scale, and the like. In parallel with these corrections, at step G and step H, the amount of correction to the projection magnification is determined from the deformation ratio of the substrate, as derived previously, and when the projection magnification has been corrected, the semiconductor substrate is exposed to light at step I.

However, this previously proposed method for correcting registration within a chip described above results in the following problems. Namely, slight adjustment of the projection magnification is carried out by changing the air pressure between the group of projecting lenses, and thus changing the refractive index

between the projecting lenses and the air. However, there are limits due to lens design on the range of adjustment of the refractive index. In concrete terms, if the projection magnification of a light exposure device using a reducing projection method is converted to the deformation ratio of a semiconductor substrate, the possible change is limited to a range of only 5 - 10 ppm or so.

Furthermore, in an equal-size light exposure device typical in equal-size X ray light exposure devices, it is, in principle, impossible to adjust the rate of magnification, and therefore any deformation occurring in a semiconductor substrate cannot be corrected in this way.

A feature of a light exposure method and light exposure device to be described, by way of example, in illustration of the present invention is that highly accurate registration within a chip can be achieved over a wide range of deformation ratios in a semiconductor substrate, regardless of the type of light exposure system used.

A particular light exposure method to be described, by way of example in illustration of the present invention includes the following steps for forming a prescribed pattern onto a semiconductor substrate.

Namely, the size of the semiconductor substrate is measured, and the difference between this measured size of the semiconductor substrate and its design size is found. Thereupon, the semiconductor substrate is heated or cooled in order to correct the semiconductor substrate to its design size. A prescribed pattern of light is then exposed onto the semiconductor substrate.

The action of the arrangement mentioned above will now be described. The temperature of a semiconductor substrate changes at each step of semiconductor fabrication. Furthermore, error may occur between the actual size of the semiconductor substrate and its design size, due to the action of the different films formed on to the surface of the semiconductor substrate. However, in the arrangement to be described, a pattern is exposed after the temperature of the semiconductor substrate has been adjusted such that any error is eliminated. Therefore, it is possible to obtain a more accurate exposure at all times.

The light exposure device to be described below, by way of example in illustration of the present invention includes a light source for shining exposure light on to the semiconductor substrate, a detector for detecting alignment marks on the semiconductor substrate, and a laser interferometer which acts as a substrate position

sensor for detecting positional information relating to the semiconductor substrate when the alignment marks are detected. The light exposure device includes a signal processing unit, which measures the size of the semiconductor substrate from the output signal of the laser interferometer and calculates the error between the measured size and the design size of the semiconductor substrate, and a temperature adjusting mechanism which heats or cools the semiconductor substrate on the basis of the output from the signal processing unit.

Arrangements illustrative of the invention will now be described by way of example with reference to Figs. 1 to 3 of the accompanying drawings in which:-

Fig. 1 is an approximate sectional view of a light exposure device relating to a first embodiment,

Fig. 2 is a flowchart for describing a light exposure method using a light exposure device relating to the first embodiment, and

Fig. 3 is an approximate sectional view of a light exposure device relating to a second embodiment.

Referring to Fig. 1, a light exposure device includes an excimer laser serving as a light source for generating exposure light L, and a stage 8 on which a semiconductor substrate 35 is mounted. The light exposure device is also provided with a detector 6. This detector

6 recognizes alignment marks previously formed on the semiconductor substrate 35, by means of an optical transceiver 7. Alignment marks are formed on the semiconductor substrate 35 in at least two positions in mutually perpendicular directions (X direction and Y direction), respectively, (a total of at least 4 positions); (as a general example of alignment marks, the configuration shown in Fig. 9 may also be used.

The light exposure device is also provided with a signal processing unit 5 and control unit 4 for determining the deformation ratio of the semiconductor substrate 35 from signals from the detector 6 and the positions of the alignment marks, as well as a holder 9 on which the semiconductor substrate 35 is mounted, and a temperature regulating fluid circulation mechanism 1 built into this holder 9. The light exposure device is further provided with a temperature sensor 2 for measuring the temperature of the semiconductor substrate 35 located in the holder 9, and a control unit 4 for providing PID control of a temperature regulator 3 on the basis of signals from the signal processing unit and temperature signals from the temperature sensor 2.

The exposure light L in this light exposure device is produced using a 248-nm wavelength excimer laser 22, for example. This excimer laser 22 emits KrF excimer

laser light which contains light of a particular frequency band only. This exposure light L is reshaped to a suitable form by means of a beam expander 21. It is then directed via a reflecting mirror 20 to a fly's eye lens 19. This fly's eye lens 19 has an array of a plurality of small lenses and is used so that a uniform exposure light L is directed onto a reticle, which is described later. The exposure light L is then reshaped by passing through an aperture stop 18 and a condenser lens 23. Finally, the exposure light L is shone uniformly on to the reticle 13. A circuit pattern is previously formed on the reticle 13. Consequently, the exposure light L having passed through the circuit pattern of the reticle 13 is reduced to a prescribed projection magnification by means of a projecting lens 12 and it is focused on the surface of the semiconductor substrate 35, on which the desired pattern is exposed.

The light exposure device includes an alignment optics system, in addition to the exposure light optics system. In this alignment optics system, laser light from a He-Ne laser 17 is directed via reflecting mirrors 15, 16 and an optical transceiver 7 onto the alignment marks formed on the semiconductor substrate 35, and positional information is gathered by means of the detector 6 detecting the diffracted light. The light used

for alignment does not have to be He-Ne laser light, and light of a broad waveband can be used to detect the images of the alignment marks. It is also possible to use the same optics system for alignment and light exposure.

The temperature regulating fluid circulation mechanism 1, which raises and lowers the temperature of the semiconductor substrate 35 is provided inside the holder 9 and is connected to the temperature regulator 3 via prescribed pipework. A temperature sensor 2 is also provided in the holder 9. The temperature sensor 2 is a high-resolution sensor, for example, one using a platinum resistor, or the like. The output signal from the temperature sensor 2 buried in the holder 9 is transmitted to the aforementioned control unit 4. The control unit 4 performs PID control of the temperature regulator 3 and allows the temperature of the semiconductor substrate 35 to reach a prescribed temperature in a short period of time. The control unit 4 incorporates a microcomputer as a PID controller.

Next, steps for measuring the actual distance between alignment marks in order to calculate the deformation ratio of the semiconductor substrate 35 are described. As stated previously, the alignment marks are formed in the X direction or Y direction of the semiconductor substrate 35. A He-Ne laser is directed

continuously from the optical transceiver 7 onto the semiconductor substrate 35. When an alignment mark on the semiconductor substrate 35 comes directly under the optical transceiver 7, this alignment mark is detected by the detector 6. The positional information relating to the semiconductor substrate 35 at this point is measured by means of a laser interferometer 11 serving as a substrate position sensor, and this information is recorded. Thereupon, the stage 8 is moved again until the next alignment mark comes under the optical transceiver 7. The position of the semiconductor substrate 35 when this alignment mark comes under the optical transceiver 7 is measured. The actual distance (length) between the alignment marks can be detected from this positional information for the semiconductor substrate 35 as measured by the laser interferometer 11. The laser interferometer actually directly measures the distance moved by the stage 8, but since the semiconductor substrate 35 is mounted on the stage 8, the distance between alignment marks can be measured accurately.

Here, it is desirable to provide at least two alignment marks each in the X and Y directions, in other words, four or more independent alignment marks in the X and Y directions, respectively, In particular, if alignment marks are provided near the outer perimeter of

the semiconductor substrate 35, then it is possible to determine the deformation ratio of the semiconductor substrate 35 by means of equation (1) and equation (2) described above. By increasing the number of alignment marks, the deformation ratio can be determined more accurately.

Next, a method for correcting errors in a light exposure pattern caused by deformation of the semiconductor substrate 35 is described with reference to Fig. 1 and Fig. 2. Fig. 2 is flowchart illustrating a light exposure method using the light exposure device shown in Fig. 1.

Firstly, at step A in Fig. 2, a semiconductor substrate 35 (wafer) is mounted on the holder 9 shown in Fig. 1, and at step B, the temperature of the semiconductor substrate 35 is measured by the temperature sensor 2. At step C, the stage 8 is moved and the semiconductor substrate 35 is aligned with the optical transceiver 7. Here, the temperature measurement step B and the alignment step C may be reversed in sequence. Next, at step D, alignment marks formed in a plurality of locations on the semiconductor substrate 35 (wafer) are detected via the optical transceiver 7 by the detector 6. At step E, the signal processing unit 5 compares the detected distance between alignment marks with the design

distance between alignment marks, which is determined previously, and calculates the deformation ratio. The error is derived and then corrected at steps F and G, respectively.

Next, a procedure for correcting error is described. Normally, the deformation dL of a material due to temperature change is found by the following equations, where α is the coefficient of thermal expansivity.

$$L = L0\ (1 + \alpha T) \quad (3)$$

$$dL = L2 - L1 = L0(1 + \alpha T2) - L0(1 - \alpha T1) \quad (4)$$

Here,

L: length of material

T: temperature

L1:length of material at temperature T1

L2:length of material at temperature T2

The deformation dL is derived from the amount of error described above, and T1 is the previously measured temperature of the semiconductor substrate 35. L0 is the theoretical distance between the alignment marks, and can be determined if information relating to the chip design specifications is provided. The coefficient of thermal expansivity α is an intrinsic value of the material, which in the case of silicon is 2.6×10^{-6}. Desirably, to correct the error more accurately, the thermal

coefficient of expansivity should be determined at each stage of film deposition and pattern formation in the semiconductor fabrication process. However, in the case of a typical 6-inch diameter silicon semiconductor substrate, the thickness of the substrate itself is approximately 700 μm, which is sufficiently large with respect to the thickness of the various films formed subsequently for there to be no great error produced if the above value is used.

Next, at step H, a target substrate temperature T2 is determined. Let us consider, for example, that the temperature of the semiconductor substrate 35 is 23°C, the design distance between alignment marks is 100 mm, and the error between the two alignment marks is −0.50 μm (the board has contracted with respect to the design values). Using equations (1) and (2), the target substrate temperature T2 can be calculated as about 24.92°C. Conversely, if the substrate has expanded with respect to the design values, then the target substrate temperature T2 could be set as about 21.08°C.

When the target substrate temperature T2 has been determined on the basis of the calculation results from control unit 4 shown in Fig. 1, at step I, the temperature of the semiconductor substrate is adjusted by the temperature regulating mechanism. Specifically, the

temperature of a fluid such as "fluorinate" (water can also be used) is controlled by the temperature regulator 3. This fluid is cycled through the holder 9 and regulates the temperature of the semiconductor substrate 35 via the holder 9. The temperature of the semiconductor substrate 35 is measured by the temperature sensor 2 and PID controlled by the control unit 4. Next, step J identifies when the temperature of the semiconductor substrate 35 has come sufficiently close, for example, within ±0.2°C, of the target substrate temperature T2, whereupon, at step K, light exposure commences. In this case, alongside the process of correcting the deformation of the semiconductor substrate 35, shift components and rotational components, etc. are also corrected. In this way, it is possible to correct error due to deformation of a semiconductor substrate accurately. As regards the temperature regulating mechanism, apart from a system using a prescribed fluid, as described above, it is also possible to adjust the temperature electrically by providing electrothermal wires, or the like, in the holder.

Furthermore, since the deformation is corrected by approximately 2.6 ppm for each 1(°C) temperature change in the case of a silicon semiconductor substrate, a temperature change of around 8°C is sufficient, even if a

correction of 20 ppm is required. A temperature change of this order will have no detrimental effect on the photoresist. Therefore, the optical reaction of the photoresist will occur without obstacle, and hence error can be corrected across a wide range of deformation ratios. The temperature of the semiconductor substrate is in the region of 20-30°C.

Fig. 3 shows an approximate sectional view of a second embodiment. As shown in Fig. 3, this light exposure device differs from the one in the first embodiment in that a temperature regulating unit 3a is provided in the course of the pipework between the temperature regulator 3 and the temperature regulating fluid circulation mechanism 1. Apart from this, the composition is the same as the light exposure device illustrated in Fig. 1.

If the temperature of the semiconductor substrate 35 is regulated by the temperature regulator 3 alone, when a plurality of semiconductor substrates are exposed, then even if PID control is used, it takes a long time to reach the target substrate temperature T2. As a result, the throughput in semiconductor manufacture declines. To avoid this, when a plurality of semiconductor substrates are being processed, from the second semiconductor substrate 35 onwards, the semiconductor substrate 35 is

first placed over the temperature regulating unit 22 and the temperature is adjusted beforehand to the region of the target substrate temperature. Thereupon, the next semiconductor substrate, which has been adjusted in temperature by the temperature regulating unit 3a, is mounted into the holder 9 and its temperature is regulated as described in the first embodiment, whereupon it is exposed.

By adjusting the temperature of the subsequent semiconductor substrate beforehand by means of the temperature regulating unit 3a, the time taken for the semiconductor substrate 35 to reach the target substrate temperature is reduced, thereby producing the merit of improved throughput in semiconductor manufacture. However, the scope of the protection sought is not limited to this, and a temperature regulating unit including electrothermal wires, or the like, may also be used.

In arrangements described above, in illustration of the present invention, the distance between alignment marks is measured and this distance is compared with a design distance to measure the error between the two. The rate of deformation of the semiconductor substrate after pre-processing is then determined, the semiconductor substrate is heated or cooled to a target substrate

temperature corresponding to this deformation ratio, and a pattern is then exposed. Therefore, advantages are obtained in that error can be corrected and highly accurate registration within a chip is possible, registration faults are reduced, and the yield rate in semiconductor manufacture is raised.

Although particular embodiments, illustrative of the invention have been described by way of example, it will be understood that variations and modifications thereof, as well as other embodiments, may be made within the scope of the protection sought by the appended claims.

The disclosure in the specification of Japanese Patent Application No. 09-005375 (Filed on January 16th, 1997) may helpfully be referred to in understanding the present invention.

CLAIMS

1. A light exposure method for forming a prescribed pattern on a semiconductor substrate, including the steps of

measuring the size of the semiconductor substrate,

determining the error between the measured size and the design size of the semiconductor substrate,

heating or cooling the semiconductor substrate in order to correct the size of the semiconductor substrate to the design size, and

exposing a prescribed pattern of light on to the semiconductor substrate.

2. A light exposure method as claimed in Claim 1, wherein the size of the semiconductor substrate is measured by measuring the distance between two or more alignment marks previously formed on the surface of the semiconductor substrate.

3. A light exposure method as claimed in Claim 2, wherein the alignment marks are formed respectively in mutually perpendicular directions on the surface of the semiconductor substrate.

4. A light exposure method as claimed in Claim 2, wherein the alignment marks are formed near to the outer perimeter of the semiconductor substrate.

5. A light exposure method as claimed in Claim 2, wherein any one of the two or more alignment marks is detected and positional information for the semiconductor substrate is recorded,

a further alignment mark is detected and further positional information for the semiconductor substrate is recorded, and

the size of the semiconductor substrate is calculated from the items of positional information.

6. A light exposure method for forming a prescribed pattern on a semiconductor substrate, including the steps of

measuring the size of the semiconductor substrate,

determining the error between the measured size and the design size of the semiconductor substrate,

detecting the temperature of the semiconductor substrate and calculating the temperature difference between this temperature and a target substrate temperature for adjusting the semiconductor substrate to its design size,

heating or cooling the semiconductor substrate on the basis of this temperature difference, and

exposing a prescribed pattern on the surface of the semiconductor substrate.

7. A light exposure method as claimed in claim 6,

wherein the size of the semiconductor substrate is measured by measuring the distance between two or more alignment marks previously formed on the surface of the semiconductor substrate.

8. A light exposure method as claimed in Claim 7, wherein the alignment marks are formed respectively in mutually perpendicular directions on the surface of the semiconductor substrate.

9. A light exposure method as claimed in Claim 7, wherein the alignment marks are formed near to the outer perimeter of the semiconductor substrate.

10. A light exposure method as claimed in Claim 7, wherein any one of the two or more alignment marks is detected and positional information for the semiconductor substrate is recorded, a further alignment mark is detected and further positional information for the semiconductor substrate is recorded,

and the size of the semiconductor substrate is calculated from the items of positional information.

11. A light exposure method for forming a prescribed pattern onto a semiconductor substrate, including the steps of

measuring the size of the semiconductor substrate,

determining the error between the measured size and the design size of the semiconductor substrate,

detecting the temperature of the semiconductor substrate,

calculating the temperature difference for heating or cooling from the error between the actual size and the design size of the semiconductor substrate and the coefficient of thermal expansivity of the semiconductor substrate,

heating or cooling the semiconductor substrate on the basis of this temperature difference in order to correct it to the design size, and

exposing a prescribed pattern on to the surface of the semiconductor substrate.

12. A light exposure method as claimed in Claim 11, wherein the size of the semiconductor substrate is measured by measuring the distance between two or more alignment marks previously formed on the surface of the semiconductor substrate.

13. A light exposure method as claimed in Claim 12, wherein the alignment marks are formed respectively in mutually perpendicular directions on the surface of the semiconductor substrate.

14. A light exposure method as claimed in Claim 12, wherein the alignment marks are formed near to the outer perimeter of the semiconductor substrate.

15. A light exposure method as claimed in Claim

12, wherein any one of the two or more alignment marks is detected and positional information for the semiconductor substrate is recorded, a further alignment mark is detected and the further positional information for the semiconductor substrate is recorded,

and the size of the semiconductor substrate is calculated from the items of positional information.

16. A light exposure device for forming a prescribed pattern on a semiconductor substrate, including

a light source for directing exposure light on to the semiconductor substrate,

a detector for detecting alignment marks formed on the semiconductor substrate,

a substrate position sensor for detecting positional information for the semiconductor substrate when an alignment mark is detected,

a signal processing unit for measuring the size of the semiconductor substrate from the output signal from the substrate position sensor, and for detecting any error between the measured size and the design size of the semiconductor substrate, and

a temperature regulating mechanism for heating or cooling the semiconductor substrate on the basis of the output from the signal processing unit.

17. A light exposure device as claimed in Claim 16, wherein the light exposure device is further provided with a temperature sensor for detecting the temperature of the semiconductor substrate.

18. A light exposure device as claimed in Claim 17, wherein the light exposure device is further provided with a control unit for calculating a heating temperature or cooling temperature on the basis of temperature information from the temperature sensor and the error in the size of the semiconductor substrate from the signal processing unit.

19. A light exposure device as claimed in Claim 16, wherein the temperature regulating mechanism include a temperature regulator for setting a prescribed temperature regulating fluid to a prescribed temperature, and a temperature regulating fluid circulation mechanism for circulating the temperature regulating fluid in the vicinity of the semiconductor substrate.

20. A light exposure device as claimed in Claim 19, wherein the temperature regulating mechanism is further provided with a temperature regulating unit which previously heats or cools the semiconductor substrate to a temperature close to the target substrate temperature, prior to the light exposure process.

21. A light exposure method as claimed in Claim 1

substantially as described herein with reference to Figs. 1 and 2 or Fig. 3 of the accompanying drawings.

22. A light exposure device as claimed in Claim 16 substantially as described herein with reference to Fig. 1 or Fig. 3 of the accompanying drawings.

The Patent Office

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Application No: GB 9800991.3
Claims searched: 1-22

Examiner: Richard Nicholls
Date of search: 27 March 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G2A (AEAA, AEE, AFX)

Int Cl (Ed.6): G03B 27/52, 27/53, 27/58 ; G03F 7/20, 9/00

Other: Online databases : WPI, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 1578259 A	(PHILIPS) See especially figure 11 and page 6 lines 85-116	1,6,11&16 at least
X	US 4720732	(CANON) see especially figure 1 and column 2 lines 10-18	1,6,11&16 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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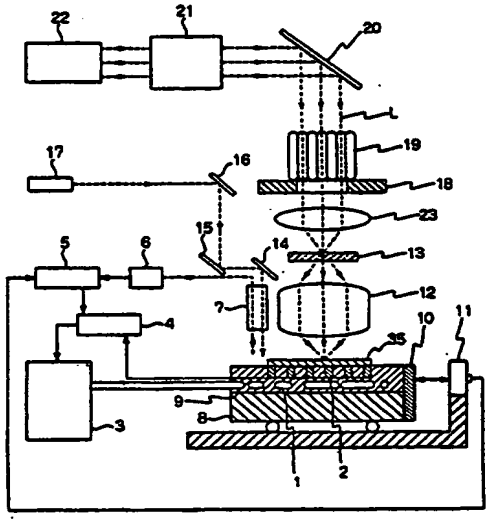
(54) Abstract Title

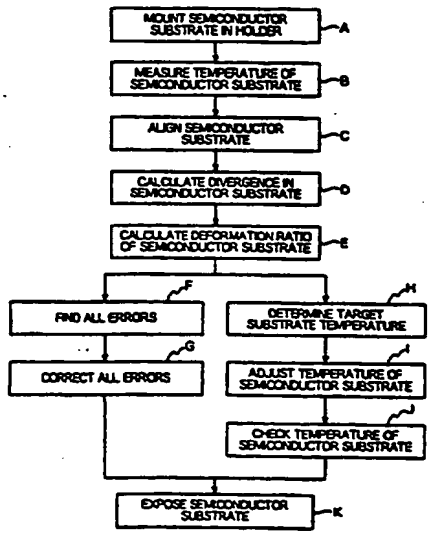
Forming a pattern on a semiconductor substrate including heating or cooling the substrate to adjust its size

(57) A light exposure method and device for forming a prescribed pattern on a semiconductor substrate 35 are described in which the size of a the semiconductor substrate is measured; any error between the measured size and the design size of the semiconductor substrate is determined; the semiconductor substrate is heated and/or cooled in order to correct the design size; and a prescribed pattern is exposed on to the semiconductor substrate. The light exposure device includes a light source for directing exposure light on to the semiconductor substrate; a detector 6 for detecting alignment marks formed on the semiconductor substrate; and a substrate position sensor 7 for detecting positional information for the semiconductor substrate when an alignment mark is detected. The light exposure device also includes a signal processing unit 5 for measuring the size of the semiconductor substrate from the output signal from the substrate position sensor, and for detecting an error between the measured size and the design size of the semiconductor substrate. The light exposure device also has a temperature regulating mechanism 1 for heating or cooling the semiconductor substrate on the basis of the output from the signal processing unit.

F I G.1



F I G.2



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